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1 Circuit design and modeling: Maximum effective distance of on-chip decoupling capacitors in power distribution grids   ■
Mikhail Popovich, Eby G. Friedman, Michael Sotman, Avinoam Kolodny, Radu M. Secareanu
April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**
Publisher: ACM Press
Full text available: 🗎 pdf(524.44 KB)   Additional Information: full citation, abstract, references, index terms

> Decoupling capacitors are widely used to reduce power supply noise. On-chip decoupling capacitors have traditionally been allocated into the available white space on a die. The efficacy of on-chip decoupling capacitors depends upon the impedance of the power/ground lines connecting the capacitors to the current loads and power supplies. A maximum effective radius exists for each on-chip decoupling capacitor. Beyond this effective distance, a decoupling capacitor is completely ineffective. Two ef ...

> **Keywords**: decoupling capacitors, power distribution grids, power distribution systems

2 Power, buffering and open source: Effects of on-chip inductance on power distribution grid   ■
Atsushi Muramatsu, Masanori Hashimoto, Hidetoshi Onodera
April 2005 **Proceedings of the 2005 international symposium on Physical design ISPD '05**
Publisher: ACM Press
Full text available: 🗎 pdf(362.07 KB)   Additional Information: full citation, abstract, references, index terms

> With increase of clock frequency, on-chip wire inductance starts to play an important role in power/ground distribution analysis, although it has not been considered so far. We perform a case study work that evaluates relation between decoupling capacitance position and noise suppression effect, and we reveal that placing decoupling capacitance close to current load is necessary for noise reduction. We experimentally show that impact of on-chip inductance becomes small when on-chip decoupling ca ...

> **Keywords**: decoupling capacitance, on-chip inductance, power distribution network, power supply noise

3 Power supply noise analysis methodology for deep-submicron VLSI chip design   ■
Howard H. Chen, David D. Ling

June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**
Publisher: ACM Press
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This paper describes a new design methodology to analyzethe on-chip power supply noise
for high-performance microprocessors.Based on an integrated package-level andchip-level
power bus model, and a simulated switching circuitmodel for each functional block, this
methodology offersthe most complete and accurate analysis of Vdd distributionfor the
entire chip. The analysis results not only providedesigners with the inductive ¿I noise and
the resistive IRdrop data at the same time, but also allow d ...

4 <u>Power-driven Design of Router Microarchitectures in On-chip Networks</u>   ▬
Hangsheng Wang, Li-Shiuan Peh, Sharad Malik
December 2003 **Proceedings of the 36th annual IEEE/ACM International Symposium**
on Microarchitecture
Publisher: IEEE Computer Society
Full text available: ▥ pdf(255.15 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>citings</u>, <u>index terms</u>

As demand for bandwidth increases in systems-on-a-chipand chip multiprocessors,
networks are fast replacing busesand dedicated wires as the pervasive interconnect fabric
foron-chip communication. The tight delay requirements facedby on-chip networks have
resulted in prior microarchitecturesbeing largely performance-driven. While performanceis
a critical metric, on-chip networks are also extremelypower-constrained. In this paper, we
investigate on-chipnetwork microarchitectures from a power-drive ...

5 <u>Energy aware design: Power protocol: reducing power dissipation on off-chip data</u>   ▬
<u>buses</u>
K. Basu, A. Choudhary, J. Pisharath, M. Kandemir
November 2002 **Proceedings of the 35th annual ACM/IEEE international symposium**
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Publisher: IEEE Computer Society Press
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Power consumption is becoming increasingly important for both embedded and high-
performance systems. Off-chip data buses can be a major power consumer In this paper,
we present a strategy called "power protocol" that tries to reduce the dynamic power
dissipation on off-chip data buses. To accomplish this, our strategy reduces the number of
bus lines that need to be activated for data transfer by employing a small cache (called
"value cache") at each side of the off-chip data bus. These value cac ...

6 <u>Low power memory system: System level power-performance trade-offs in</u>   ▬
<u>embedded systems using voltage and frequency scaling of off-chip buses and</u>
<u>memory</u>
Kiran Puttaswamy, Kyu-Won Choi, Jun Cheol Park, Vincent J. Mooney, Abhijit Chatterjee,
Peeter Ellervee
October 2002 **Proceedings of the 15th international symposium on System Synthesis**
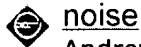**Publisher:** ACM Press

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In embedded systems, off-chip buses and memory (i.e., L2 memory as opposed to the L1
memory which is usually on-chip cache) consume significant power, often more than the
processor itself. In this paper, for the case of an embedded system with one processor
chip and one memory chip, we propose frequency and voltage scaling of the off-chip

buses and the memory chip and use a known micro-architectural enhancement called a store buffer to reduce the resulting impact on execution time. Our benchmark ...

Keywords: design space, embedded systems, power-performance trade-offs, voltage/frequency scaling

7 Power Grid and Signal Integrity Analysis: Scaling trends of on-chip Power distribution noise
Andrey V. Mezhiba, Eby G. Friedman
April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction**
Publisher: ACM Press
Full text available: pdf(110.79 KB)   Additional Information: full citation, abstract, references, citings, index terms

The design of power distribution networks in high performance integrated circuits has become significantly more challenging with recent advances in process technology. As on-chip currents exceed tens of amperes and circuit clock periods are reduced well below a nanosecond, the signal integrity of the on-chip power supply has become a primary concern in integrated circuit design. The existing work on power distribution noise scaling is reviewed and extended to include the scaling of the inductanc ...

Keywords: power distribution, power supply noise, technology scaling

8 System design methodology: Replacing global wires with an on-chip network: a power analysis
Seongmoo Heo, Krste Asanović
August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**
Publisher: ACM Press
Full text available: pdf(250.91 KB)   Additional Information: full citation, abstract, references, index terms

This paper explores the power implications of replacing global chip wires with an on-chip network. We optimize network links by varying repeater spacing, link pipelining, and voltage scaling, to significantly reduce the energy to send a bit across chip. We develop an analytic model of large chip designs with an on-chip two-dimensional mesh network and estimate the power savings possible in a 70 nm process for two different design points: a circuit-switched ASIC or FPGA design, and a dynamic pack ...

Keywords: on-chip network power model, pipelining, router, tile size, tiled architecture, wire power model

9 Leakage estimation: Full chip leakage estimation considering power supply and temperature variations
Haihua Su, Frank Liu, Anirudh Devgan, Emrah Acar, Sani Nassif
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(1.15 MB)   Additional Information: full citation, abstract, references, citings, index terms

Leakage power is emerging as a key design challenge in current and future CMOS designs. Since leakage is critically dependent on operating temperature and power supply, we present a full chip leakage estimation technique which accurately accounts for power

supply and temperature variations. State of the art techniques are used to compute the thermal and power supply profile of the entire chip. Closed-form models are presented which relate leakage to temperature and VDD variations. These models c ...

Keywords: leakage power, supply voltage variation, thermal analysis

10 Managing power and performance for System-on-Chip designs using Voltage Islands ▬

David E. Lackey, Paul S. Zuchowski, Thomas R. Bednar, Douglas W. Stout, Scott W. Gould, John M. Cohn

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

Full text available: 🔒 pdf(96.51 KB)   Additional Information: full citation, abstract, references, citings, index terms

This paper discusses Voltage Islands, a system architecture and chip implementation methodology, that can be used to dramatically reduce active and static power consumption for System-on-Chip (SoC) designs. As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption.Effectiv ...

11 Low power SOCs and NOCs: High-level power analysis for on-chip networks ▬

Noel Eisley, Li-Shiuan Peh

September 2004 **Proceedings of the 2004 international conference on Compilers, architecture, and synthesis for embedded systems**

Publisher: ACM Press

Full text available: 🔒 pdf(353.56 KB)   Additional Information: full citation, abstract, references, index terms

As on-chip networks become prevalent in multiprocessor systems-on-a-chip and multi-core processors, they will be an integral part of the design flow of such systems. With power increasingly the primary constraint in chips, the tool chain in systems design, from simulation infrastructures to compilers and synthesis frameworks, needs to take network power into account, motivating the need for early-stage communication power analysis.While there has been substantial research in network performance ...

Keywords: link utilization, power analysis, simulation, systems-on-a-chip (SoC)

12 Poster Session 1: FIFO power optimization for on-chip networks ▬

Sudarshan Banerjee, Nikil Dutt

April 2004 **Proceedings of the 14th ACM Great Lakes symposium on VLSI**

Publisher: ACM Press

Full text available: 🔒 pdf(105.29 KB)   Additional Information: full citation, abstract, references, index terms

As the design community moves towards architecting multiprocessor systems-on-chip (MPSoC), it is widely believed that an on-chip interconnection network is potentially the best candidate to satisfy the high aggregate throughput needed by dozens of IP blocks. In this context, power (energy) estimation and reduction techniques for switches and links, the core components of an interconnection network, gain added significance. FIFO buffers are a key component of a majority of network switches - buff ...

Keywords: FIFO, low power design, on-chip networks, shared memory, switches, wide flits

13 An experimental system for power/timing optimization of LSI chips   ▬

B. J. Agule, J. D. Lesser, A. E. Ruehli, P. K. Wolff

January 1977 **Proceedings of the 14th conference on Design automation**

Publisher: IEEE Press

Full text available: 🔄 pdf(423.02 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

An experimental system of programs is described which places logic gates on a chip, globally wires the gates and then optimizes the power required to drive them. Further power reductions are realized by using power-oriented placement improvement techniques. A companion paper describes how the optimization is accomplished by using the timing requirements of the chip as constraints and assigning delays to the logic gates so that these constraints are met and the power is minimized.

14 Power distribution issues: Macro-modeling concepts for the chip electrical interface   ▬

◈ Brian W. Amick, Claude R. Gauthier, Dean Liu

June 2002 **Proceedings of the 39th conference on Design automation**

Publisher: ACM Press

Full text available: 🔄 pdf(515.95 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

The power delivery network is made up of passive elements in the distribution network, as well as the active transistor loads. A chip typically has three types of power supplies that require attention: core, I/O, and analog. Core circuits consist of digital circuits and have the largest current demand. In addition to all of the system issues/models for the core, modeling the I/O subsystem has the additional requirement of modeling return paths and discontinuities. The analog circuits present yet ...

Keywords: VLSI power distribution, analog and I/O power delivery, high speed microprocessor design, inductance

15 Clock, power grid and thermal analysis and optimization: Fast computation of the   ▬

◈ temperature distribution in VLSI chips using the discrete cosine transform and table look-up

Yong Zhan, Sachin S. Sapatnekar

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: 🔄 pdf(1.25 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>

Temperature-related effects are critical in determining both the performance and reliability of VLSI circuits. Accurate and efficient estimation of the temperature distribution corresponding to a specific circuit layout is indispensable in physical design automation tools. In this paper, we propose a highly accurate fast algorithm for computing the on-chip temperature distribution due to power sources located on the top surface of the chip. The method is a combination of several computational te ...

16 Power-performance considerations of parallel computing on chip multiprocessors   ▬

◈ Jian Li, José F. Martínez

December 2005 **ACM Transactions on Architecture and Code Optimization (TACO),**
Volume 2 Issue 4

Publisher: ACM Press

Full text available: 🔄 pdf(565.90 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

This paper looks at the power-performance implications of running parallel applications on chip multiprocessors (CMPs). First, we develop an analytical model that, for the first time, puts together parallel efficiency, granularity of parallelism, and voltage/frequency scaling,

to establish a formal connection with the power consumption and performance of a parallel code running on a CMP. We then conduct detailed simulations of parallel applications running on a detailed power-performance CMP mod ...

Keywords: Voltage/frequency scaling, granularity, parallel efficiency

17 <u>Compiler-directed channel allocation for saving power in on-chip networks</u>

Guangyu Chen, Feihui Li, Mahmut Kandemir

January 2006 **ACM SIGPLAN Notices , Conference record of the 33rd ACM SIGPLAN-SIGACT symposium on Principles of programming languages POPL '06,**
Volume 41 Issue 1

Publisher: ACM Press

Full text available: <u>pdf(943.11 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

Increasing complexity in the communication patterns of embedded applications parallelized over multiple processing units makes it difficult to continue using the traditional bus-based on-chip communication techniques. The main contribution of this paper is to demonstrate the importance of compiler technology in reducing power consumption of applications designed for emerging multi processor, NoC (Network-on-Chip) based embedded systems. Specifically, we propose and evaluate a compiler-directed a ...

Keywords: NoC, compiler, energy consumption

18 <u>Power grid, thermal, and leakage issues: The need for a full-chip and package thermal model for thermally optimized IC designs</u>

Wei Huang, Eric Humenay, Kevin Skadron, Mircea R. Stan

August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**

Publisher: ACM Press

Full text available: <u>pdf(1.08 MB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

Modeling and analyzing detailed die temperature with a full-chip thermal model at early design stages is important to discover and avoid potential thermal hazards. However, omitting important aspects of *package* details in a thermal model can result in significant temperature estimation errors. In this paper, we discuss the applications of an existing compact thermal model that models both *die* and *package* temperature details. As an example, a thermally self-consistent leakage ...

Keywords: leakage, package, temperature-aware design, thermal model

19 <u>Model and analysis for combined package and on-chip power grid simulation</u>

Rajendran Panda, David Blaauw, Rajat Chaudhry, Vladimir Zolotov, Brian Young, Ravi Ramaraju

August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**

Publisher: ACM Press

Full text available: <u>pdf(220.58 KB)</u>   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

We present new modeling and simulation techniques to improve the accuracy and efficiency of transient analysis of large power disðtribution grids. These include an accurate model for the inherent decoupling capacitance of non-switching devices, as well as a staðtistical switching current model for the switching devices. Moreðover, three new simulation techniques are presented for problem size-reduction and speed-up. Results of

application of these techöniques on three PowerPCtm

20 On-chip communication architectures: analysis and optimisation: Power analysis of
◈ system-level on-chip communication architectures
Kanishka Lahiri, Anand Raghunathan
September 2004 **Proceedings of the 2nd IEEE/ACM/IFIP international conference on
Hardware/software codesign and system synthesis**
Publisher: ACM Press
Full text available: 🅰 pdf(101.16 KB)   Additional Information: full citation, abstract, references, index terms

For complex System-on-chips (SoCs) fabricated in nanometer technologies, the system-
level on-chip communication architecture is emerging as a significant source of power
consumption. Managing and optimizing this important component of SoC power requires a
detailed understanding of the characteristics of its power consumption.Various power
estimation and low-power design techniques have been proposed for the global
interconnects that form part of SoC communication architectures (*e.g.*, low- ...

Keywords: communication architectures, low-power design, network-on-chip, power
analysis, system-on-chip

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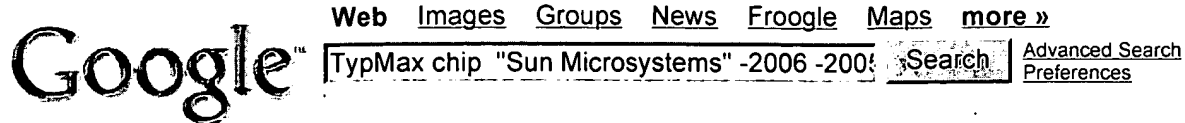   Preferences

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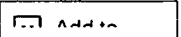|	Type	L #	Hits	Search Text	DBs	Time Stamp
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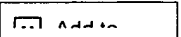Add terms to your search using: `AND` ⊠

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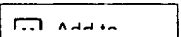   <u>1 result</u>   `⊡ Add to`
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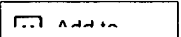   <u>48 results</u>   `⊡ Add to`
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